4. (Amended) Apparatus as claimed in claim 1, wherein said translator output signals include control signals that control operation of said processor core and specify parameters not specified by control signals produced on decoding instructions of said first instruction set.

5. (Amended) Apparatus as claimed in claim 1, wherein said restart logic is part of said instruction translator.

6. (Amended) Apparatus as claimed in claim 1, wherein said restart logic stores a pointer to a restart location within instructions of said second instruction set that are being translated, said pointer being advanced upon execution of said final operation.

8. (Amended) Apparatus as claimed in claim 1, wherein instructions of said second instruction set specify operations to be executed upon stack operands held in a stack and said input variables include input stack operands.

10. (Amended) Apparatus as claimed in claim 8, wherein any stack operands added to said stack by execution of said at least one instruction of said second instruction are not added until after execution of said final operation has commenced.

11. (Amended) Apparatus as claimed in claim 1, wherein said input variables include system state variables not specified within said second instruction.

12. (Amended) Apparatus as claimed in claim 1, wherein said processor has a register bank containing a plurality of registers and instructions of said first instruction set execute operations upon register operands held in said registers.

15. (Amended) Apparatus as claimed in claim 1, wherein said instructions of said second instruction set are Java Virtual Machine instructions.